

CLAIMS

What is claimed is:

1           1.     An I/O interface for an integrated circuit chip having a core, a pad,  
2     and a data buffer disposed between the core and the pad, the data buffer  
3     comprising:

4                 an output circuit including:

5                     a plurality of output latches, each output latch having at least  
6                         one input coupled to receive output data signals from  
7                         the core;

8                     a plurality of output clock trees, each output clock tree  
9                         coupled to at least one of the output latches for  
10                         triggering the latching of the output data signals from  
11                         the core, each output clock tree disposed in the I/O  
12                         interface;

13                     a first signal conditioning circuit coupled to the output latches  
14                         for conditioning the output data signals so that the  
15                         output data signals are compliant with at least one of a  
16                         plurality of protocols;

17                 an input circuit including:

18                     a plurality of input latches, each input latch having at least one  
19                         input coupled to receive input data signals from the  
20                         pad;

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21 an input clock tree coupled to at least one of the input latches  
22 for triggering the latching of the input data signals from  
23 the pad; and  
24 a second signal conditioning circuit coupled to the input  
25 latches for conditioning the input data signals so that  
26 the input data signals are compliant with at least one of  
27 the plurality of protocols:

1 2. The I/O interface of claim 1, wherein the input clock tree distributes  
2 to the data buffer a clock/strobe signal generated from a source external to the  
3 I/O interface.

1 3. The I/O interface of claim 1, wherein the output data signals and the  
2 input data signals are conditioned by the first signal conditioning circuit and the  
3 second signal conditioning circuit, respectively, to be compliant with a protocol  
4 that is selected on-the-fly.

1 4. The I/O interface of claim 3, wherein the protocol is selected from  
2 the group of protocols consisting of AGP, DDR/SSTL, and PCI/TTL.

1 5. The I/O interface of claim 4, wherein the data buffer operates in a  
2 synchronous mode for AGP and DDR/SSTL protocols, and the data buffer  
3 operates in an asynchronous mode for PCI/TTL protocol.

1           6.     The I/O interface of claim 1, wherein the output circuit includes a  
2     first output latch, a second output latch, and a third output latch, the first output  
3     latch and the second output latch each coupled to a first output clock tree, the  
4     third output latch coupled to a second output clock tree, the output clock trees  
5     for triggering the latching of the output data signals from the core in a  
6     synchronous manner.

1           7.     The I/O interface of claim 6, wherein the first clock tree provides a  
2     double rate clock and the second clock tree provides a single rate clock.

1           8.     The I/O interface of claim 6, wherein the first output latch, the  
2     second output latch, and the third output latch are edge-triggered flip-flops.

1           9.     The I/O interface of claim 1, wherein the first signal conditioning  
2     circuit comprises:

3                   a pre-driver having an input and an output, the input coupled  
4                   to the output latches for receiving the output data  
5                   signals;

6                   a voltage tolerant circuit having an input and an output, the  
7                   input coupled to the output of the pre-driver for  
8                   receiving output data signals; and

9                   a driver circuit having an input and an output, the input  
10                  coupled to the output of the voltage tolerant circuit for  
11                  receiving the output data signals, the output of the

12 driver circuit coupled to the pad for providing a pad  
13 voltage compliant with one of the plurality of protocols.

1 10. The I/O interface of claim 9, wherein the voltage tolerant circuit is  
2 further coupled to the pad via a switching well, the switching well operating in  
3 conjunction with the voltage tolerant circuit and the driver circuit to compare the  
4 pad voltage with a supply voltage and switching the higher of the two voltages  
5 to the switching well.

1 11. The I/O interface of claim 10, wherein the switching well is further  
2 coupled to a pull-up/pull-down circuit for adjusting the pad voltage.

1 12. The I/O interface of claim 11, wherein the pull-up/pull-down circuit  
2 includes a pull-up resistor and a pull-down resistor, each resistor responsive to  
3 an enabling signal from the core.

1 13. The I/O interface of claim 1, wherein the input circuit includes a first  
2 input latch, a second input latch, and a third input latch, each input latch coupled  
3 to the input clock for triggering the latching of the input data signals from the  
4 pad in a synchronous manner.

1 14. The I/O interface of claim 1, wherein the input circuit includes a  
2 Schmitt trigger coupled to the pad for receiving input data signals compliant  
3 with PCI/TTL protocol.

1        15.    The I/O interface of claim 1, wherein the input circuit includes a  
2    differential amplifier coupled to the pad for receiving differential input data  
3    signals.

1        16.    An I/O interface for an integrated circuit chip having a core, a pad,  
2    and a clock/strobe buffer disposed between the core and the pad, the  
3    clock/strobe buffer comprising:

4                    a differential amplifier having an input and an output, the  
5                    input coupled to the pad for receiving differential  
6                    clock/strobe signals complying with one of a plurality  
7                    of protocols;  
8                    a programmable delay module having inputs and an output, a  
9                    first input coupled to the output of the differential  
10                    amplifier for receiving the clock/strobe signals, a  
11                    second input for receiving a plurality of program bits  
12                    for delaying the clock/strobe signals; and  
13                    a gated buffer coupled to the output of the programmable  
14                    delay module and an input clock tree, the gated buffer  
15                    for distributing the clock/strobe signals to the I/O  
16                    interface via the input clock tree.

1        17.    The I/O interface of claim 16, wherein the protocol is selected from  
2    the group of protocols consisting of AGP and DDR/SSTL.

1 18. The I/O interface of claim 16, wherein the clock/strobe buffer  
2 further includes a Schmitt trigger coupled to the pad and the gated buffer for  
3 receiving TTL clock/strobe signals from the pad and distributing the TTL  
4 clock/strobe signals to the I/O interface via the input clock tree.

1 19. An I/O interface for an integrated circuit chip having a core, a pad,  
2 and a clock/strobe buffer disposed between the core and the pad, the  
3 clock/strobe buffer comprising:

4 an output circuit including:

5 an output latch having at least one input coupled to receive  
6 output clock/strobe signals from the core, the output  
7 latch coupled to a first clock tree for triggering the  
8 latching of the output clock/strobe signals from the  
9 core, the first output clock tree disposed in the I/O  
10 interface;

11 a multiplexer having at least one input coupled to a second  
12 clock tree, the multiplexer for reducing the skew on the  
13 clock/strobe signals, the second output clock tree  
14 disposed in the I/O interface;

15 a first signal conditioning circuit coupled to the output latch  
16 and the multiplexer for conditioning the output  
17 clock/strobe signals so that the output clock/strobe  
18 signals are compliant with at least one of a plurality of  
19 protocols;

20 an input circuit including:  
21 a differential amplifier having an input and an output, the  
22 input coupled to the pad for receiving differential  
23 clock/strobe signals complying with one of a plurality  
24 of protocols; and  
25 a gated buffer coupled to the output of the differential  
26 amplifier and an input clock tree, the gated buffer for  
27 distributing the clock/strobe signals via the input clock  
28 tree .

1 20. The I/O interface of claim 19, wherein the protocol is selected from  
2 the group of protocols consisting of AGP and DDR/SSTL.

1 21. The I/O interface of claim 19, wherein the clock/strobe buffer  
2 further includes a Schmitt trigger coupled to the pad and the gated buffer for  
3 receiving TTL clock/strobe signals from the pad and distributing the  
4 clock/strobe signals to the I/O interface via the input clock tree.